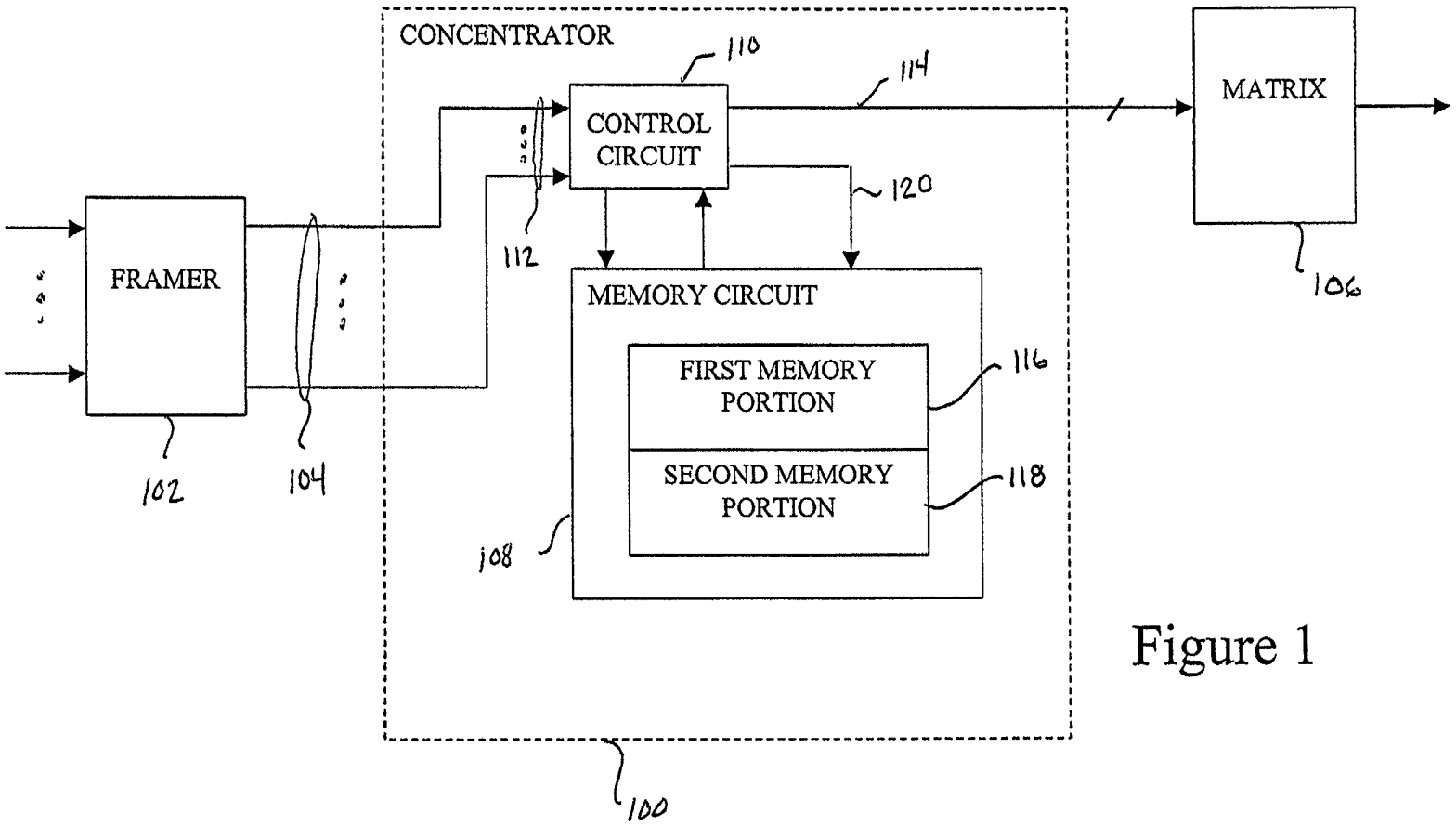
CONCENTRATOR
110
114
CONTROL CIRCUIT
MATRIX
120
FRAMER
112
MEMORY CIRCUIT
FIRST MEMORY PORTION
116
SECOND MEMORY PORTION
118
108
102
104
106
100

Figure 1

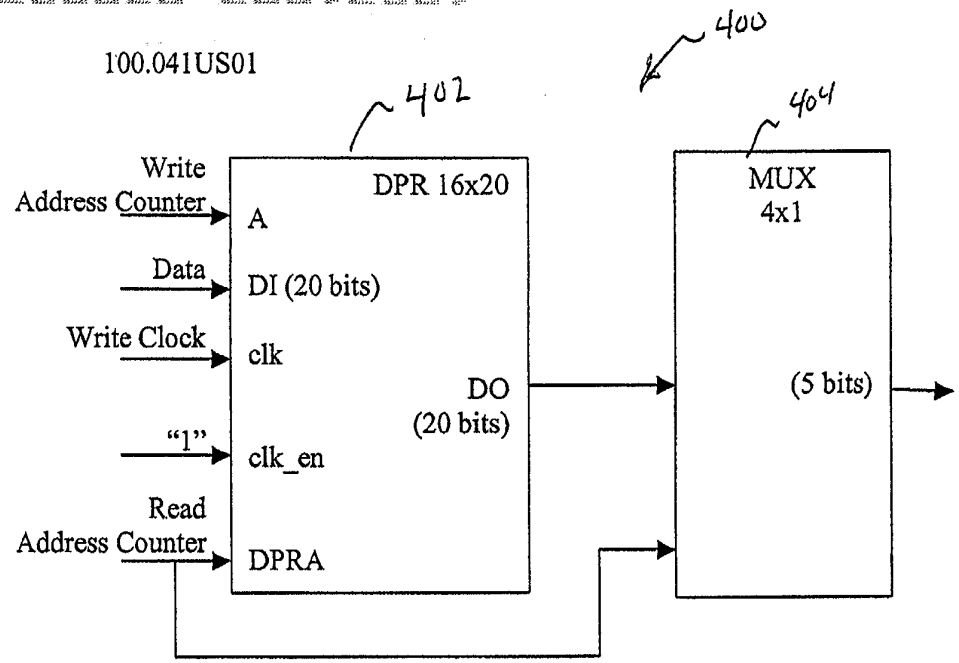

Figure 4

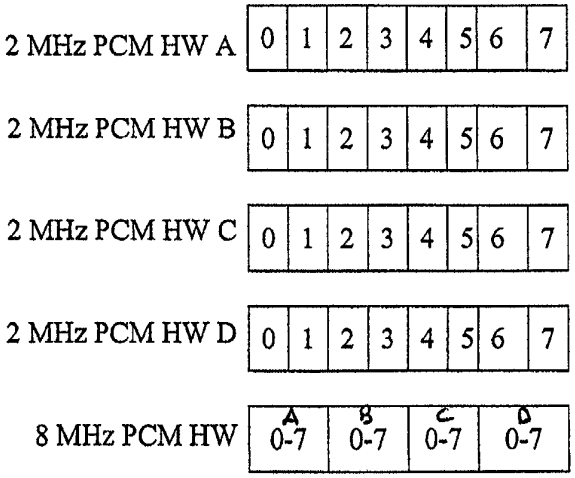

Figure 2

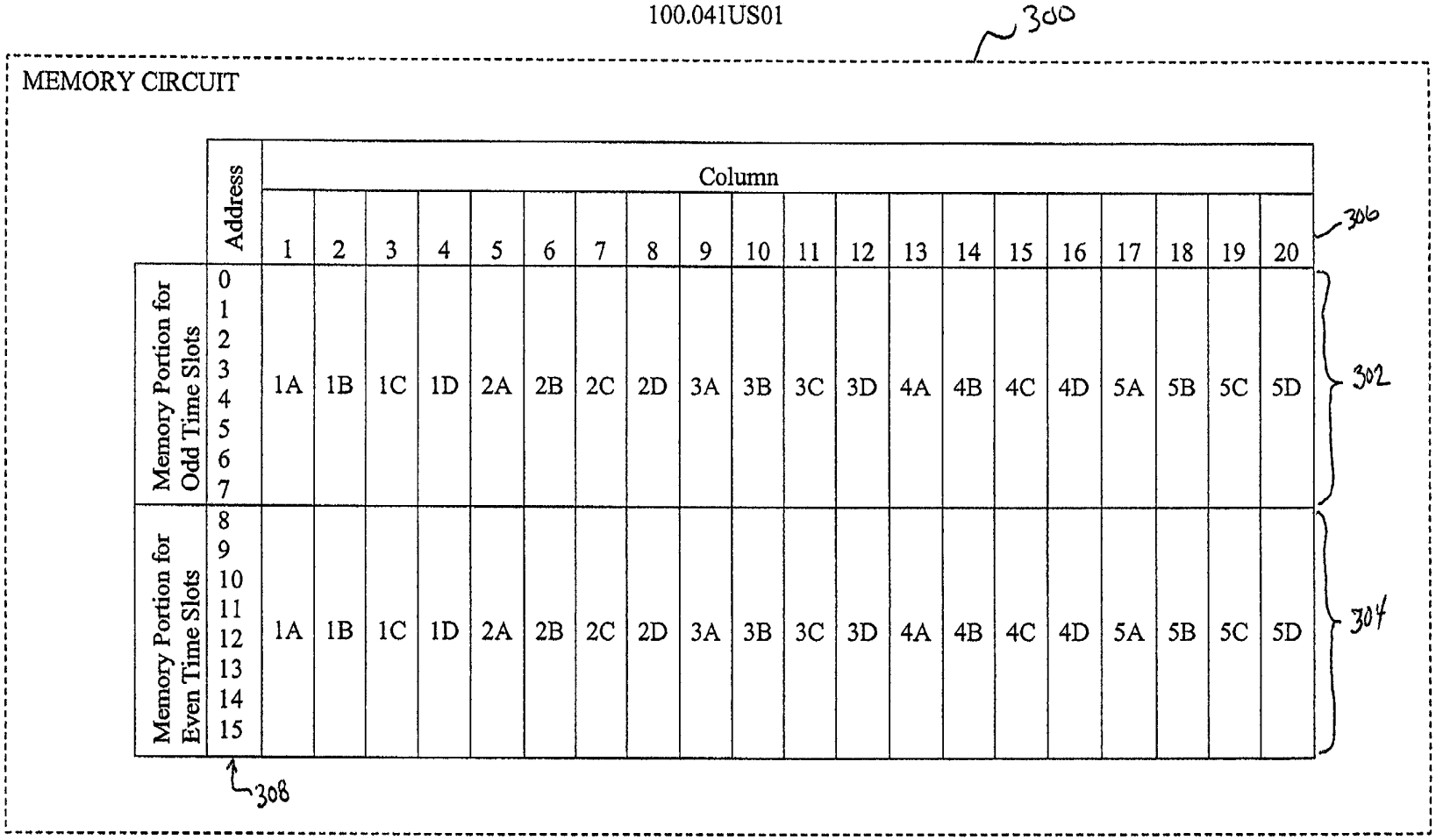
300
MEMORY CIRCUIT
Address
Column
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
306
Memory Portion for Odd Time Slots
0 1 2 3 4 5 6 7
1A 1B 1C 1D 2A 2B 2C 2D 3A 3B 3C 3D 4A 4B 4C 4D 5A 5B 5C 5D
302
Memory Portion for Even Time Slots
8 9 10 11 12 13 14 15
1A 1B 1C 1D 2A 2B 2C 2D 3A 3B 3C 3D 4A 4B 4C 4D 5A 5B 5C 5D
304
308

Figure 3

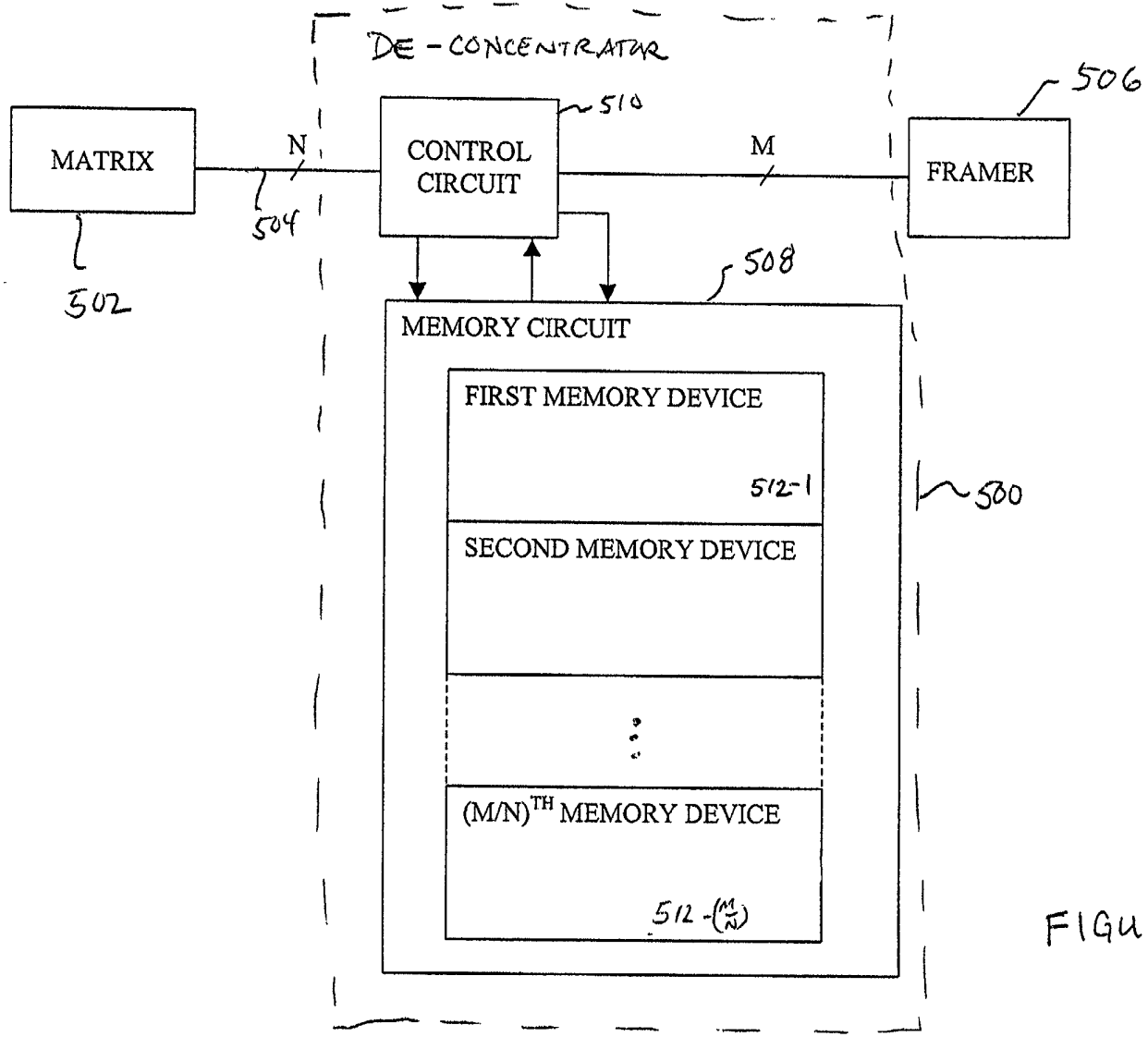
DE-CONCENTRATOR
MATRIX
N
504
CONTROL CIRCUIT
510
M
FRAMER
506
502
508
MEMORY CIRCUIT
FIRST MEMORY DEVICE
512-1
500
SECOND MEMORY DEVICE
(M/N)TH MEMORY DEVICE
512-(M/N)

FIGURE 5

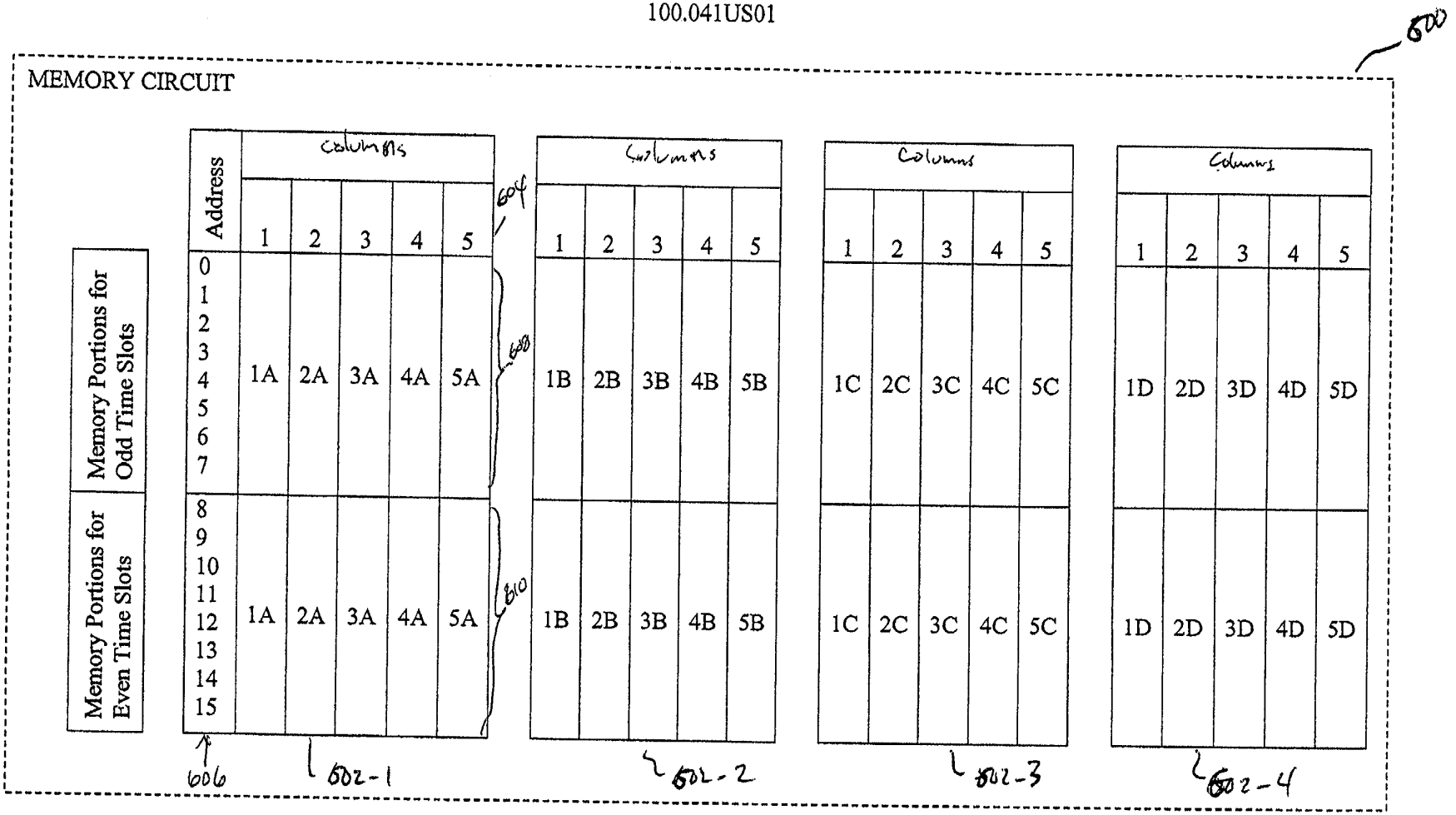
600
MEMORY CIRCUIT
Memory Portions for Odd Time Slots
Memory Portions for Even Time Slots
Address
Columns
1 2 3 4 5
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
1A 2A 3A 4A 5A
1B 2B 3B 4B 5B
1C 2C 3C 4C 5C
1D 2D 3D 4D 5D
604
608
610
606
602-1
602-2
602-3
602-4

Figure 6

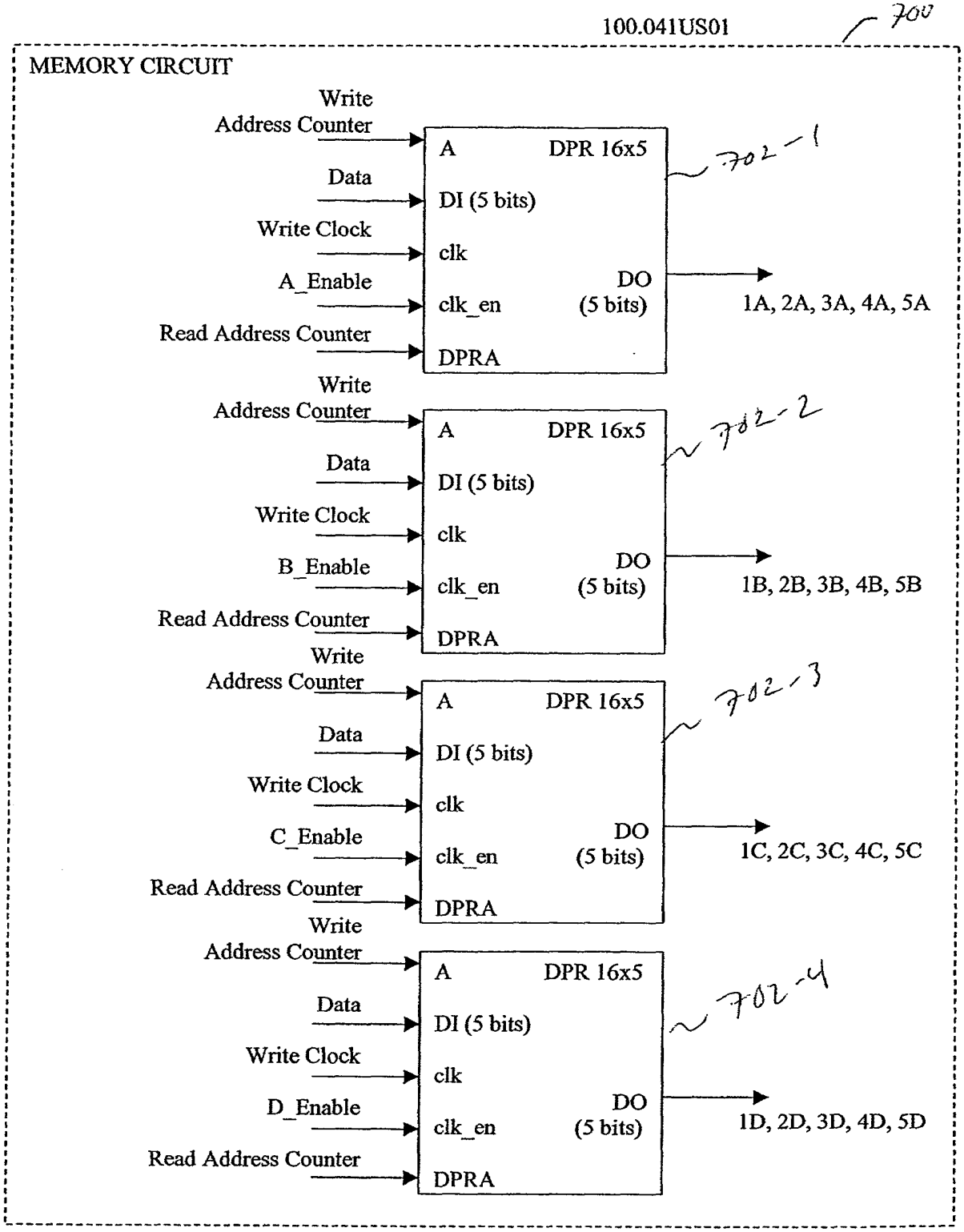
700
MEMORY CIRCUIT
Write Address Counter
Data
Write Clock
A_Enable
Read Address Counter
A
DI (5 bits)
clk
clk_en
DPRA
DPR 16x5
DO (5 bits)
702-1
1A, 2A, 3A, 4A, 5A
Write Address Counter
Data
Write Clock
B_Enable
Read Address Counter
A
DI (5 bits)
clk
clk_en
DPRA
DPR 16x5
DO (5 bits)
702-2
1B, 2B, 3B, 4B, 5B
Write Address Counter
Data
Write Clock
C_Enable
Read Address Counter
A
DI (5 bits)
clk
clk_en
DPRA
DPR 16x5
DO (5 bits)
702-3
1C, 2C, 3C, 4C, 5C
Write Address Counter
Data
Write Clock
D_Enable
Read Address Counter
A
DI (5 bits)
clk
clk_en
DPRA
DPR 16x5
DO (5 bits)
702-4
1D, 2D, 3D, 4D, 5D

Figure 7